



Paper id: 251024

Printed Page: 1 of 2
Subject Code: BEC063

Roll No:

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BTECH
(SEM VI) THEORY EXAMINATION 2024-25
CMOS DIGITAL DESIGN TECHNIQUE

TIME: 3 HRS

M.MARKS: 70

Note: Attempt all Sections. In case of any missing data; choose suitably.

SECTION A**1. Attempt all questions in brief.****02 x 7 = 14**

Q no.	Question	CO	Level
a.	Define wafer preparation and lithography in VLSI fabrication.	CO1	K1
b.	Explain the significance of threshold voltage in a MOSFET.	CO1	K2
c.	Differentiate between enhancement and depletion MOSFETs.	CO1	K2
d.	What is trans conductance in MOSFETs?	CO2	K2
e.	Explain lambda-based design rule in CMOS layout.	CO2	K1
f.	Calculate propagation delay of a CMOS inverter with output capacitance 10fF and ON resistance 5kΩ.	CO4	K3
g.	What is the function of sense amplifier in SRAM?	CO5	K1

SECTION B**2. Attempt any three of the following:****07 x 3 = 21**

a.	Explain CMOS n-well fabrication process with diagram.	CO1	K2
b.	Derive threshold voltage equation for MOSFET and discuss affecting factors.	CO2	K3
c.	Design CMOS inverter and analyze its voltage transfer characteristics.	CO4	K3
d.	Compare pseudo-NMOS logic and transmission gate logic with circuits.	CO4	K4
e.	Explain working of Schmitt trigger circuit and its applications.	CO5	K3

SECTION C**3. Attempt any one part of the following:****07 x 1 = 07**

a.	Explain second-order effects (DIBL, CLM, Body Effect) in MOSFETs.	CO2	K4
b.	Discuss scaling effects in CMOS technology on power, speed and density.	CO2	K4

4. Attempt any one part of the following:**07 x 1 = 07**

a.	Derive noise margin expressions for CMOS inverter and explain significance.	CO4	K3
b.	Design 2-input NAND gate using CMOS and analyze power dissipation.	CO4	K3

5. Attempt any one part of the following:**07 x 1 = 07**

a.	Explain dynamic CMOS logic circuit working with example and advantages.	CO4	K4
b.	Design D-latch using transmission gates and explain operation.	CO5	K3



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6. Attempt any one part of the following:

07 x 1 = 07

a.	Explain 6T SRAM cell operation with diagram. Difference from DRAM.	CO5	K3
b.	Discuss ASIC design flow and compare full-custom vs semi-custom approaches.	CO5	K4

7. Attempt any one part of the following:

07 x 1 = 07

a.	Calculate average dynamic power dissipation of CMOS inverter with 20fF load at 100MHz if rise time is 2ns.	CO4	K3
b.	Explain row and column decoder circuit in memory design with diagram.	CO5	K3

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