PAPER ID-310262

Subject Code: KEC072

Roll No: | | | | | | | | | | | | | |

BTECH
(SEM VII) THEORY EXAMINATION 2024-25
VLSI DESIGN

TIME: 3 HRS **M.MARKS: 100**

Note: Attempt all Sections. In case of any missing data; choose suitably.

SECTION A

1. Attempt *all* questions in brief. **2 x 10 = 20**

Q no.	Question	CO	Level
a.	Define Moore's Law.	1	K1
b.	Explain the importance of critical path analysis in VLSI design.	1	K2
c.	What is skin effect?	2	K1
d.	Compare the transient response of a lumped and distributed RC model.	2	K4
e.	What is charge sharing in dynamic CMOS circuits?	3	K1
f.	Explain the cascading of dynamic gates	3	K2
g.	Differentiate between DRAM and SRAM.	4	K2
h.	List the types of non-volatile memories.	4	K1
i.	Explain controllability and observability in testing.	5	K2
j.	Define fault in the context of digital circuits.	5	K1

SECTION B

2.	**Attempt any *three* of the following:**	**10 x 3 = 20**	
a.	Illustrate the VLSI design hierarchy and describe the layers of abstraction with examples.	1	K3
b.	Analyze the effects of resistance, capacitance, and inductance on interconnect performance in the distributed RC model.	2	K4
c.	Explain the noise considerations in dynamic CMOS design and their impact on performance.	3	K2
d.	Define DRAM and SRAM and describe their basic operation principles.	4	K1
e.	Explain ad-hoc technique for testability in a combinational circuit.	5	K2

SECTION C

3.	**Attempt any *one* part of the following:**	**10 x 1 = 10**	
a.	Analyze the impact of CMOS propagation delay on circuit performance, incorporating the concept of sheet resistance.	1	K4
b.	Define the critical path in VLSI design and explain its significance in timing analysis.	1	K1
4.	**Attempt any *one* part of the following:**	**10 x 1 = 10**	
a.	Derive the RC delay model for a given interconnect circuit and calculate its transient response.	2	K3
b.	List and explain the parameters affecting interconnects in VLSI circuits.	2	K1
5.	**Attempt any *one* part of the following:**	**10 x 1 = 10**	
a.	Analyze the problems associated with single-phase clocking in dynamic CMOS circuits.	3	K4
b.	Describe the steady-state behavior of dynamic CMOS gate circuits.	3	K1
6.	**Attempt any *one* part of the following:**	**10 x 1 = 10**	
a.	Explain the differences between volatile and non-volatile memories with examples.	4	K2
b.	Analyze the power consumption in CMOS circuits and the impact of voltage scaling on power efficiency.	4	K4
7.	**Attempt any *one* part of the following:**	**10 x 1 = 10**	
a.	Define common faults in digital circuits and their impact on circuit behavior.	5	K1
b.	Analyze the functional modeling of faults at the logic and register levels.	5	K4