



Roll No:

BTECH**(SEM. VI) THEORY EXAMINATION 2025-26****CMOS DIGITAL DESIGN TECHNIQUE****TIME: 3 HRS****M.MARKS: 70****Note:** Attempt all Sections. In case of any missing data; choose suitably.**SECTION A****1. Attempt all questions in brief.****02 x 7 = 14**

Q. no.	Question	CO	Level
a.	Define VLSI design flow.	1	K1
b.	Outline the differences between an enhancement MOSFET and a depletion MOSFET.	1	K2
c.	Explain transconductance in a MOS transistor.	2	K2
d.	What is a stick diagram in CMOS layout design?	2	K1
e.	Explain the propagation delay in a CMOS inverter.	3	K2
f.	Define pseudo NMOS logic.	4	K1
g.	Illustrate the differences between SRAM and DRAM.	5	K2

SECTION B**2. Attempt any three of the following:****07 x 3 = 21**

a.	Explain the structure and operation of the MOS transistor with suitable diagrams.	1	K5
b.	Discuss MOSFET current-voltage characteristics for different operating regions.	2	K6
c.	Explain the limitations of CMOS technology in nanoscale circuit design.	3	K5
d.	Design of a Boolean function $F = ABC + \overline{A}C + B\overline{C}$ using transmission gate logic.	4	K6
e.	Discuss and implement a NOR-based SR latch circuit using CMOS logic.	5	K6

SECTION C**3. Attempt any one part of the following:****07 x 1 = 07**

a.	Discuss different VLSI design styles and compare: (i) Full custom design (ii) Semi-custom design (iii) FPGA-based design	1	K6
b.	Explain the CMOS n-well fabrication process with neat cross-sectional diagrams.	1	K6

4. Attempt any one part of the following:**07 x 1 = 07**

a.	Design a CMOS inverter layout using the stick diagram approach and explain layout optimization techniques. A MOS transistor has: • Width 20 μm • Length 2 μm Determine the aspect ratio and comment on its effect on drain current.	2	K6
b.	Explain lambda-based CMOS design rules with suitable examples.	2	K5



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(SEM. VI) THEORY EXAMINATION 2025-26

CMOS DIGITAL DESIGN TECHNIQUE

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5. Attempt any *one* part of the following: 07 x 1 = 07

a.	Derive the propagation delay expression for the CMOS inverter and discuss factors affecting delay.	3	K6
b.	Explain the operation and transfer characteristics of a CMOS inverter with a neat diagram.	3	K5

6. Attempt any *one* part of the following: 07 x 1 = 07

a.	Explain pull-up and pull-down network realization and analyze design parameters. Design a CMOS combinational circuit for: $Y = \overline{(A + B + C)} \cdot D$	4	K6
b.	Discuss dynamic logic circuit design and compare it with static CMOS logic.	4	K6

7. Attempt any *one* part of the following: 07 x 1 = 07

a.	Discuss CMOS <i>D</i> latch flip flop realization in detail.	5	K6
b.	Discuss SRAM and DRAM cell design with suitable diagrams.	5	K6