

Roll No:

BTECH
(SEM. VI) THEORY EXAMINATION 2025-26
DIGITAL DESIGN AND VHDL

TIME: 3 HRS

M.MARKS: 70

Note: Attempt all Sections. In case of any missing data; choose suitably.

SECTION A

1. Attempt all questions in brief. 02 x 7 = 14

Q no.	Question	CO	Level
a.	Why are setups and hold times important in digital circuits?	CO1	K2
b.	Define sequential circuit timing.	CO1	K1
c.	What is a multiplexer?	CO2	K1
d.	Define signal and variable in VHDL.	CO2	K2
e.	What is meant by signed number multiplication?	CO3	K2
f.	What is meant by programmable gate array architecture?	CO4	K2
g.	Define baud rate in UART communication.	CO5	K1

SECTION B

2. Attempt any three of the following: 07 x 3 = 21

Q no.	Question	CO	Level
a.	Design a synchronous sequential circuit using Mealy model to detect the sequence "101". Draw state diagram and state table.	CO1	K3
b.	Write VHDL descriptions for JK flip-flop and synchronous counter. Explain their working.	CO2	K3
c.	Explain the architecture and working of ROM, PLA and PAL with suitable diagrams.	CO3	K2
d.	Compare FPGA and CPLD on the basis of architecture, speed, power consumption and applications.	CO4	K4
e.	Discuss serial communication using UART and explain baud rate, parity bit and stop bit.	CO5	K2

SECTION C

3. Attempt any one part of the following: 07 x 1 = 07

Q no.	Question	CO	Level
a.	Explain combinational logic circuits and discuss different types of hazards in combinational networks with suitable examples.	CO1	K2
b.	Discuss timing issues in sequential circuits and explain clock skew, propagation delay, setup time and hold time.	CO1	K4

4. Attempt any one part of the following: 07 x 1 = 07

Q no.	Question	CO	Level
a.	Write and explain VHDL code for a 4-to-1 multiplexer and 3-to-8 decoder.	CO2	K3
b.	Explain the basic structure of a VHDL program with suitable syntax and examples.	CO2	K2

5. Attempt any one part of the following: 07 x 1 = 07

Q no.	Question	CO	Level
a.	Discuss the design of binary divider and explain the division algorithm with example.	CO3	K4



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b.	Design and explain a serial binary adder with block diagram and timing sequence.	CO3	K3
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6. Attempt any one part of the following:**07 x 1 = 07**

Q no.	Question	CO	Level
a.	Discuss testing techniques for combinational logic circuits with suitable examples.	CO4	K2
b.	Explain scan testing method for sequential logic circuits and discuss its advantages.	CO4	K2

7. Attempt any one part of the following:**07 x 1 = 07**

Q no.	Question	CO	Level
a.	Explain the design of a microcontroller CPU with suitable block diagram.	CO5	K3
b.	Design a simple CPU architecture for basic arithmetic and logical operations.	CO5	K6